TDAQ Global Firmware
WBS 6.8.3

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Meeting with Institute Contacts
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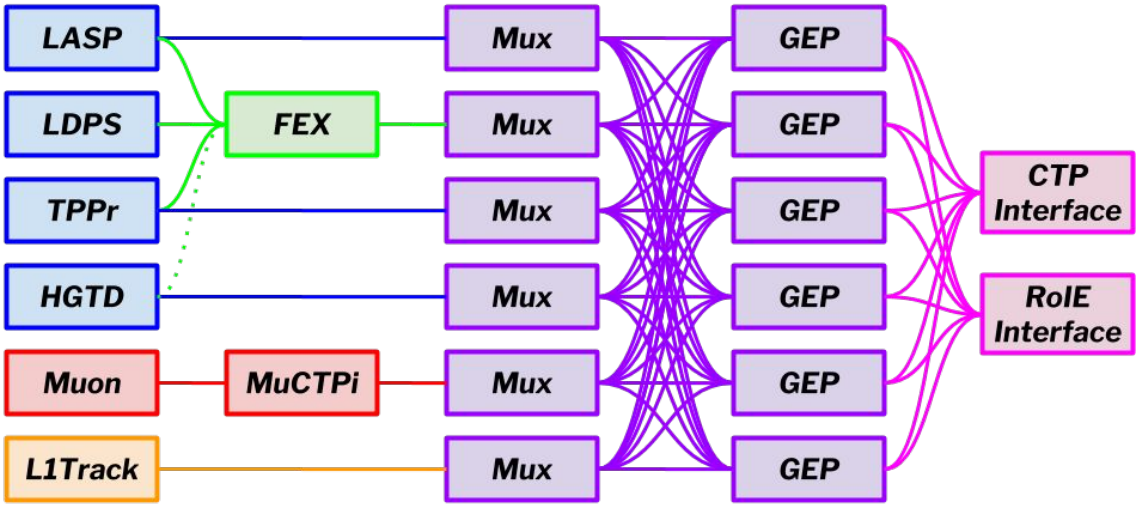
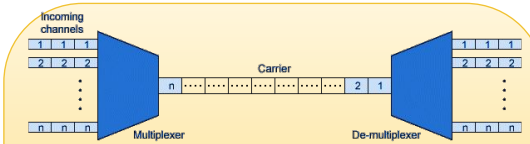
Global Hardware Proposal (MB, DS)

Serial-to-Time Multiplexed Architecture

- ***Maximize physics potential by concentrating event data in a single location***
  - **requires one system to transport data and one to process event**
  - serial data (per BC) sent to Global Trigger are time multiplexed by a Multiplexer board (Mux)
  - Mux transports data to one of many Global Event Processors (GEP) to run trigger algorithms
  - GEP interface with CTP & RoIE (via Demultiplexer?)
  - **all interfaces under discussion**





Serial-to-Time Multiplexing

- N inputs in 1 BC → 1 output in N BC
- input multiplicity driven by latency
- output multiplicity driven by number of data sinks
- inputs & outputs can have different link speeds

L0 & L1 trigger within same electronics module

https://indico.cern.ch/event/622489/contributions/2511065/attachments/1434734/2205741/20170328_TDAQ_Global_Trigger_Overview.pdf

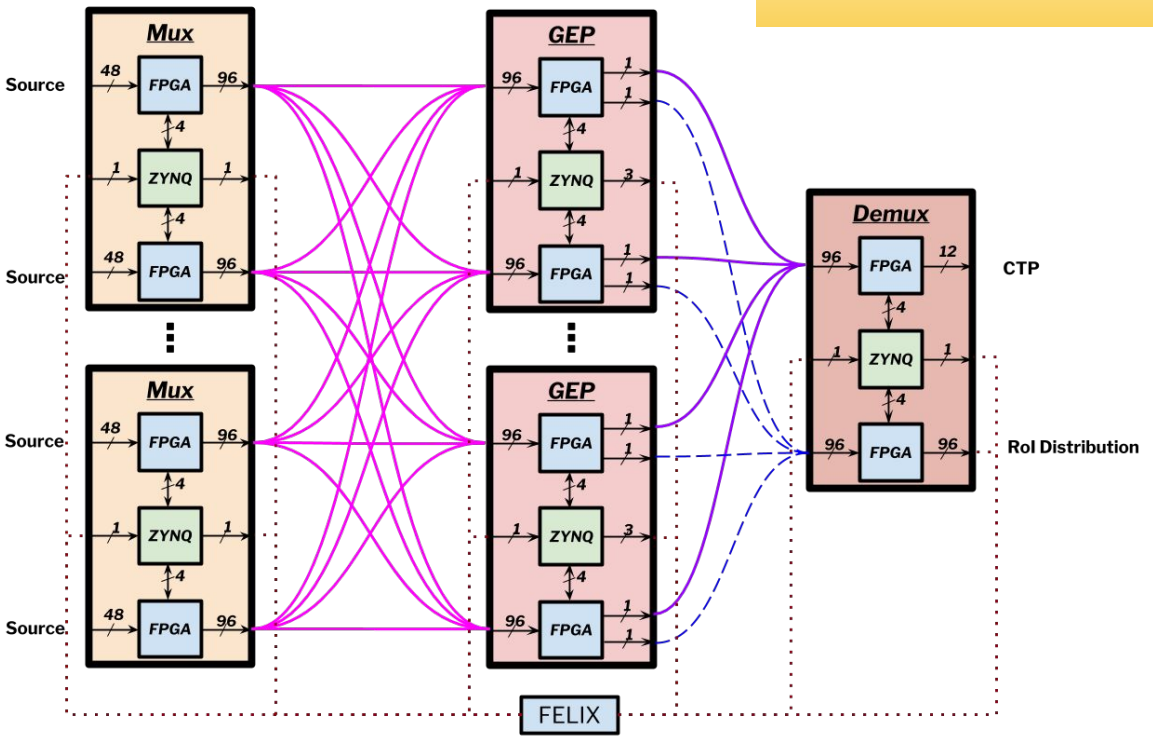
Global Hardware Proposal (MB, DS)

Global Trigger Common Module

C2104 shown in diagram

B2104 has less capacity (72 Mux) but lower cost & power

- ***Multiple variations in consideration but a single design covers all functionality***
  - Virtex Ultrascale+ FPGA
    - C2104 footprint has up to 104 MGT
    - VU5P/VU7P/VU9P/VU13P
  - Event Processor (GEP)
    - **max 96 GEP units → max 96 Mux units**
    - 2 GEP/Module → max 48 GEP Modules
  - Multiplexer (Mux)
    - 2 Mux/Module → max 48 Mux Modules
    - **max 96 input fibers/Mux → 9216 total input fibers**
  - Demultiplexer (Demux)
    - 12 outputs to CTP
    - **up to 96 outputs for RoI distribution**



FELIX
max 97 downlinks (TTC)
max 193 uplinks

Michael Begel

https://indico.cern.ch/event/622489/contributions/2511065/attachments/1434734/2205741/20170328_TDAQ_Global_Trigger_Overview.pdf

Proposal for Firmware Organization (1)

- Suggest a "master" firmware task called **Trigger Framework** firmware (a la L1Topo) [*proposal: MSU*]
  - hosted on the Global Event Processor modules (MUX fw separate)
  - firmware needs to be able to adapt to menu changes
  - responsible for monitoring, buffering, synchronization, keeping track of trigger objects, resource management
  - lesson learned from L1Topo: challenging task, should develop in parallel with hardware
- Algorithm firmware modules (including non-US scope) will then plug into this framework; natural host for integration
  - topoclustering, jet-finding, pileup suppression, electron ID, tau ID, etc…
- Define NSF scope boundary as after incoming data is unpacked into memory until it is repacked for transmission
  - DOE scope FW is all "low-level" fw (frame, i/o, control, etc)

Proposal for Firmware Organization (2)

- See additional document from Stefano Veneziano
- Firmware development will be scrutinized much more closely than in the past (lessons learned from L1Topo, FTK)
- Integration is expected to happen progressively

- Trigger framework task will help address these concerns
- Even if an algorithm slips, it will be decoupled from running remaining algorithms in the trigger system
- Flexibility to adjust timing individual algorithm development to match budget profile, if needed

Proposal for Firmware Organization (3)

- WBS organization:
  - trigger framework, integration (MSU)
  - topoclustering (Oregon, MSU)
  - jet-finding (Indiana)
  - hadronic reco (Chicago)
  - pileup suppression (Pitt)

Strategy for Task Lists

- Need good synchronization with hardware
  - however, realities of DOE vs NSF budget profiles may make this a challenge
- Hardware development stages (MB dates):
  - R&D [through Q3 2017]
  - Initial Design Review: Q4 2017
  - Design (demonstrator) [through Q2 2019]
  - Preliminary Design Review: Q3 2019
  - Prototype v1 [through Q4 2020]
  - Prototype v2 [through Q4 2021], Integration test
  - Final Design Review: Q1 2022
  - Prototype v3 [through Q4 2022], Integration test
  - Production Readiness Review: Q4 2022
  - 10% boards at CERN, Integration test [Q2 2023]
  - Green light for full production: end Q3 2023
  - All boards at CERN: end Q4 2023

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NSF PDR: Q3 2017

topo, jet-finding R&D

trigger framework IDR: Q4 2019

v1 trigger framework fw

trigger framework FW FDR ~Q1 2022

v2 trigger framework fw

algorithm FDR ~Q4 2022

v3 trigger framework fw

"PRR" for trigger framework fw

prod trigger framework fw

Next Steps

- Converge (w/ DOE HW scope) on milestone dates, scope boundary
- Develop trigger framework fw task list (SM, WF)
- Determine scope of “hadronic reco” and “pileup suppression” algorithm development (DM, TMH)